Abstract of the Disclosure:

A planar filter has a monolithic construction in order to suppress parasitic capacitances between signal electrodes and many signal pins which are led through a carrier and which each have a capacitor with a signal layer connected to the signal pin, a ground layer connected to ground and a dielectric layer separating the two layers. The electrodes of the capacitors are applied to the carrier, which forms the dielectric, is shaped as a block from a mass of a higher dielectric constant and, after shaping and perforation, is sintered and ground. The ground electrode covers the entire surface area of one of the side surfaces of the carrier, apart from pin lead-throughs of the signal pins and their surrounding area. The signal electrodes on the other side surface of the carrier form insular regions extending from the pin lead-throughs of the signal pins to the edge of the carrier. This planar filter, advantageously provided with a supporting plate, is used, for example, in plug-in connectors soldered onto printed circuit boards. A multi-pole angle-connecting device with a planar filter is also provided.

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